What is claimed is:

1. An arithmetic circuit comprising:

a first selector to which one input data and a fixed data are inputted wherein these data are selectively outputted in response to a control signal;

a second selector to which another input data and an output data of a register are inputted wherein these data are selectively outputted in response to the control signal;

an adder for receiving an output signal of the first selector and an output signal of the second selector to execute an addition of the output signals of the first and second selectors; and

a register for receiving an output signal of the adder to hold the output signal in synchronization with a clock signal.

2. An arithmetic circuit comprising:

a first selector to which one input data and a fixed data are inputted wherein these data are selectively outputted in response to a control signal;

a second selector to which another input data and an output data of a register are inputted wherein these data are selectively outputted in response to the control signal;

an inverter circuit for receiving the control signal and outputting an inverted signal thereof;

an adder for receiving an output signal of the first selector and an output signal of the second selector at its addition input terminals, and an output signal of the inverter circuit at its carry input terminal to execute an addition of the output signals of the first and second selectors and the output signal of the inverter circuit; and

a register for receiving an output signal of the adder to hold the output signal in synchronization with a clock signal.

3. An arithmetic circuit comprising:

a first latch circuit for receiving one input data to allow one input data to pass therethrough when a control signal is valid while holding one input data when the control signal is invalid;

a second latch circuit for receiving another input data to allow another input data to pass therethrough when the control signal is valid while holding another input data when the control signal is invalid;

an adder for receiving an output signal of the first latch circuit and an output signal of the second latch circuit to execute an addition of the output signals of the first and second latch circuits; and

a register for receiving an output signal of the adder and holding the output signal in synchronization with a clock signal.